Analytical CV

Tsormpatzoglou Andreas

Ph.D. Νανο-Ηλεκτρονική

M. Sc. Φυσική Υλικών

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Personal Info

Surname: Tsormpatzoglou

First Name: Andreas

Father's Name: Athanasios

Mother's Name: Anna

Birth date: 10 October 1978

Place of Birth: Thessaloniki

Marital status: Married

e-mail: atsormpa@uoi.com

Telephone: +30 6946464891

Academic Degrees

2005 - 2009	**PhD Thesis** under joint supervision between the universities: Aristotle University of Thessaloniki and Institut National Polytechnique de Grenoble. Topic: "Characterization and development of models for nanoscale multi-gate MOSFET transistors." For the first time, a PhD thesis was completed in the Department of Physics at Aristotle University of Thessaloniki under joint supervision, following a process approved by the Ministry of Education (Government Gazette 67/22-1-2008, part B). During the PhD, the time was equally divided between the French and Greek institutions, according to the signed agreements (main and supplementary). The doctoral committee included members from both institutions as well as external reviewers. As per usual practice, two degrees were awarded, one Greek and one French, with the same title, while the thesis was written and presented in English. The thesis received the grade "Excellent" from both Aristotle University of Thessaloniki and Institut National Polytechnique de Grenoble.
2002 - 2004	**Master diploma** in Material Physics, Aristotle University of Thessaloniki.
1997 - 2002	**Bachelor degree** in Physics, Physics Department, Aristotle University of Thessaloniki.

Work experience

My working experience can be divided in 4 sectors:

1. Tenure as an Assistant Professor on probation at a University,
2. Participation in research projects,
3. Work as an electronic device engineer in companies, and
4. Teaching as a laboratory associate at a Technological Educational Institute (TEI).

As an Assistant Professor on probation, I serve in the Department of Informatics and Telecommunications at the University of Ioannina, based in Arta, with a subject area of "Non-linear optical nanostructure devices for optical communication systems." In the department, I have taught four undergraduate courses and co-teach one graduate course. I have supervised 10 undergraduate theses focused on wireless telecommunications and am currently supervising one graduate thesis from the department's postgraduate program and one PhD candidate.

I have worked on research projects for a total of approximately 108 months, 29 of which were before obtaining my PhD (excluding the 3-year duration of the PENED project, which was my primary funding during my PhD) and 59 months after my PhD. The research interests I covered in the projects I participated in fall into two categories:

The study of optical nanostructure devices such as Schottky diodes with embedded quantum dots and InGaZnO TFTs for use in flexible displays.

The study of nanodevices with MOSFET structures, including multi-gate, FD-SOI, and junctionless MOSFETs.

During my PhD, I worked for a total of approximately 18 months in France, and after completing my PhD, I worked for 20 months in the USA (Lehigh University, Bethlehem, PA), where I conducted postdoctoral research within the corresponding program. At Lehigh University, I systematically studied, with electrical characterization measurements and electrical and mechanical stress tests, InGaZnO TFTs and developed a large number of wafers, both InGaZnO and Cu2O, in the clean room in an effort to create transparent p-type semiconductors for use in integrated circuits for flexible displays.

As an electronic device engineer, I worked for 18 months on a fixed-term contract at CEA-LETI (Grenoble, France), mainly studying the self-heating problems of FD-SOI MOSFETs, but also addressing many other high-tech issues such as variability and reliability of various types of transistors, with a focus on the degradation phenomena of gate oxide quality under the application of AC electrical stress.

As a laboratory associate, I taught for one semester at the Technological Educational Institute (TEI) of Serres, teaching the "Physics Lab 1" course in three departments.

It is noted that throughout my career to date, during my PhD and after, I have worked for a total of 56 months outside of Greece.

ΔΙΔΑΚΤΙΚΗ ΕΜΠΕΙΡΙΑ

10/2021 ως 04/2024	Assistant Professor on probation, in the Department of Informatics and Telecommunications, at the University of Ioannina, with a subject area of 'Non-linear optical nanostructure devices for optical communication systems.' Teaching the following courses: 2.1 Telecommunication Networks 2.2 Telecommunication Systems 2.3 Principles of Electromagnetism and Telecommunications.
10/2022 ως 04/2024	Assistant Professor on probation, in the Department of Informatics and Telecommunications, at the University of Ioannina, with a subject area of 'Non-linear optical nanostructure devices for optical communication systems.' Teaching the following courses:

	2.4 Optical Communications – Waveguides
10/2024 ως 02/2024	Assistant Professor on probation, in the Department of Informatics and Telecommunications, at the University of Ioannina, in the Postgraduate Program 'Informatics and Networks.' Co-teaching the mandatory graduate course: 1. Next Generation Telecommunication Networks.
10/2022 ως 06/2023	Assistant Professor on probation, in the Department of Informatics and Telecommunications, at the University of Ioannina, in the Postgraduate Program 'Informatics and Networks.' Co-teaching the graduate course: 2.1 Telecommunication Networks.
10/2010 ως 02/2011:	Laboratory associate for one semester in the departments of Mechanical Engineering, Civil Engineering, and Informatics and Telecommunications, teaching the course: 2.1 Physics Lab 1 in each department.

Participation in Research Programs

1. **09/2021 ως 12/2022**	Research work within the framework of the direct assignment project by FACEBOOK (META) "Development of a model oriented for mLED display screens." Scientific Supervisor: Mr. Charalampos Dimitriadis (AUTH)

2. **06/2019 ως 01/2021**	Research work within the framework of the direct assignment project by FACEBOOK "TCAD characterization and modeling of RGB LEDs." Scientific Supervisor: Mr. Charalampos Dimitriadis (AUTH)
3. **03/2015 ως 10/2015**	Research work within the framework of the project "NanoWireMemory – 3D Silicon Nanowire Memory Devices." Scientific Supervisor: Mr. Pascal Normand (Research Center DEMOKRITOS)
4. **08/2014 ως 02/2015**	Research work within the framework of the project "SYNERGIA II NANOTRIM - Continues Transistor Sizing Toolset for Nanoscale IC Optimization." Scientific Supervisor: Mr. Spyridon Nikolaidis (AUTH)
5. **02/2012 ως 08/2014**	02/2012 to 08/2014 – Research work within the framework of the project "Thin-film semiconductor oxide transistors for flexible large-scale CMOS electronics." Scientific Supervisor: Mr. Charalampos Dimitriadis (AUTH)
6. **01/2011 ως 02/2012**	Ερευνητική εργασία στα πλαίσια του προγράμματος «Νανο-τρανζίστορ MOSFET πολλαπλών πυλών: Συμπαγή μοντέλα ρεύματος και θορύβου-Ανάπτυξη εργαλείων αυτοματοποιημένου σχεδιασμού νανο-ηλεκτρονικών». Επιστημονικός Υπεύθυνος: κ. Δημητριάδης Χαράλαμπος (ΑΠΘ)
7. **01/2007 ως 12/2007**	01/2011 to 02/2012 – Research work within the framework of the project "Multi-gate MOSFET nanotransistors: Compact current and noise models – Development of automated design tools for nanoelectronics." Scientific Supervisor: Mr. Charalampos Dimitriadis (AUTH)

8. **07/2005 ως 07/2008**	PhD thesis work within the framework of the PENED 2003 program, titled "Study of ballistic MOSFET nanotransistors and thin-film microcrystalline silicon transistors for industrial production." Scientific Supervisor: Mr. Charalampos Dimitriadis (AUTH)
9. **02/2005 ως 08/2005**	Research work within the framework of the project "Development and characterization of semiconductor silicide β-FeSi2 nanocrystals on silicon." Scientific Supervisor: Mr. Charalampos Dimitriadis (AUTH)
10. **01/2003 ως 10/2003**	Research work and administrative support within the framework of the project "ePhys: Towards an effective use of ICT for Open Learning in Teaching of Physics." Scientific Supervisor: Mr. Evripidis Hatzikraniotis (AUTH)

Work in Companies

05/2016 ως 11/2017	Work as an electronic device engineer at CEA-LETI (Grenoble, France) under a fixed-term 18-month contract (CDD).

Submitted and To-Be-Submitted Research Programs

A/A	ACTION	ΣΥΜΜΕΤΟΧΗ	ΚΑΤΑΣΤΑΣΗ
1	H.F.R.I. (Hellenic Foundation for Research and Innovation) "Funding of Basic Research" (Horizontal	Scientific Supervisor	It was graded with an A but was not funded.

	support of all Sciences) ID 16618 – Subproject 1 (2022)		
2	2nd H.F.R.I. Call for the Procurement of High-Value Research Equipment (2023)	Scientific Supervisor	It was graded with an A but was not funded.
3	3rd H.F.R.I. Call for Research Projects to Support Faculty Members and Researchers (2024)	Scientific Supervisor	Submitted
4	SUB4: "Trust in Our Stars" (2024)	Member	Submitted

Summer Schools - Conference Attendance

2006: Summer School MIGAS «Emerging silicon devices for the end of the roadmap», *AUTRANS-GRENOBLE, France (Duration: 80 hours).*

2007: Summer School MIGAS «Multi-Physics and Multiscale Simulation for Nano-Electronics», *AUTRANS-GRENOBLE, France (Duration: 80 ώρες).*

2003	XX Πανελλήνιο Συνέδριο Φυσικής της Στερεάς Κατάστασης. Poster presentation.
2006	EUROSOI 2006, "Second Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits" *GRENOBLE, France. Conference Attendance.*
2007	Ultimate Integration on Silicon 2007, Παρουσίαση Αφίσας.
2008	Micro&Nano2007, "Micro- Nanoelectronics, Nanotechnology and MEMs". Oral presentation.
2010	Micro&Nano2010, "Micro- Nanoelectronics, Nanotechnology and MEMs". Oral presentation..
2012	MELECON 2012, 16th IEEE Mediterranean Electrochemical Conference. Oral presentation..

2012	MIEL 2012 28th International Conference on Microelectronics. Oral and poster presentation.
2014	International Conference on Microelectronics, ICM, 2014. Oral and poster presentation.
2023	Micro Nano 2023, 10th International Conference on Micro-Nanoelectronics, nanotechnology and MEMS. Poster presentation.
2023	37ο Πανελλήνιο Συνέδριο Φυσικής Στερεάς Κατάστασης και Επιστήμης Υλικών. Poster presentation.

Distinctions

2008: Excellence Scholarship from the Research Committee of Aristotle University of Thessaloniki as the best new PhD graduate from the Department of Physics at AUTH for the year 2008.

2022: Teaching Award for the academic year 2021-2022 from the Department of Informatics and Telecommunications at the University of Ioannina, based on the evaluation results of undergraduate students.

Scientific Recognition

Reviewer for more than 50 papers in various international scientific journals, including:

1) IEEE Transactions on electron devices

2) IEEE Electron device letters

3) Solid-State Electronics

4) Physica E: Low-Dimensional Systems and Nanostructures

5) Microelectronics Reliability

6) Advanced Science Letters

7) Microelectronic Engineering

8) Applied Physics Letters

Scientific Works

1. PhD Thesis: "Characterization and development of models for nanoscale multi-gate MOSFET transistors."
2. Master's Thesis: "Study of good and bad conductor mixtures using impedance spectroscopy measurements."
3. Undergraduate Thesis: "Golden ratio, Fibonacci numbers, and Quasicrystals."

Publication Analysis

According to the reputable website Scopus (24/04/2024), the publications are analyzed as follows: https://www.scopus.com/authid/detail.uri?authorId=9639312000

- Total number: 51
- Total citations: 887
- h index (citations): 18
- Total citations (all authors excluded):737
- h index (ετεροαναφορών) (all authors excluded): 17
- Analysis of the journals with the most publications (May 2024)

Journal	Number of publications	IF	Citescore
IEEE Transactions On Electron Devices	12	3.1	5.4
Solid State Electronics	9	1.7	3.3
Journal Of Applied Physics	6	3.2	5.1
IEEE Electron Device Letters	4	4.9	8.2
Microelectronic Engineering	3	2.3	5.5
Semiconductor Science And Technology	3	1.9	3.9

Publications in International Scientific Journals and Conferences with Peer Review

[1] A. Tsormpatzoglou, N. A. Hastas, D. H. Tassis, C. A. Dimitriadis, G. Kamarinos, P. Frigeri, et al., "Low-frequency noise spectroscopy in Au/n-GaAs Schottky diodes with InAs quantum dots," Applied Physics Letters, vol. 87, pp. 1-3, // 2005.

[2] N. Arpatzanis, A. Tsormpatzoglou, C. A. Dimitriadis, K. Zekentes, N. Camara, and M. Godlewski, "Electrical and low frequency noise properties of H-SiC p +-n-n + junction diodes," Physica Status Solidi (A) Applications and Materials Science, vol. 203, pp. 2551-2557, // 2006.

[3] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, L. Dózsa, N. G. Galkin, D. L. Goroshko, et al.,

"Deep levels in silicon Schottky junctions with embedded arrays of B-FeSi2 nanocrystallites," Journal of Applied Physics, vol. 100, // 2006.

[4] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, P. Frigeri, S. Franchi, E. Gombia, et al., "Stress-induced local trap levels in Au/n-GaAs Schottky diodes with embedded InAs quantum dots," IEEE Electron Device Letters, vol. 27, pp. 320-322, // 2006.

[5] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Kamarinos, P. Frigeri, S. Franchi, et al., "Noise spectroscopy of localized states in Au/n-GaAs Schottky diodes containing InAs quantum dots," Solid-State Electronics, vol. 50, pp. 340-344, // 2006.

[6] N. Arpatzanis, A. Tsormpatzoglou, C. A. Dimitriadis, J. D. Song, W. J. Choi, J. I. Lee, et al., "Effect of rapid thermal annealing on the noise properties of InAs/GaAs quantum dot structures," Journal of Applied Physics, vol. 102, // 2007.

[7] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, Q. Rafhay, G. Pananakakis, and G. Ghibaudo, "Semi-analytical modeling of short-channel effects in Si and Ge symmetrical double-gate MOSFETs," IEEE Transactions on Electron Devices, vol. 54, pp. 1943-1952, // 2007.

[8] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, G. Pananakakis, and G. Ghibaudo, "Semi-analytical modelling of short channel effects in Si double gate, tri-gate and gate all-around MOSFETs," Physica Status Solidi (C) Current Topics in Solid State Physics, vol. 5, pp. 3605-3608, // 2008.

[9] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, G. Pananakakis, and G. Ghibaudo, "Semianalytical modeling of short-channel effects in lightly doped silicon trigate MOSFETs," IEEE Transactions on Electron Devices, vol. 55, pp. 2623-2631, // 2008.

[10] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, G. Pananakakis, and G. Ghibaudo, "Threshold voltage model for short-channel undoped symmetrical double-gate MOSFETs," IEEE Transactions on Electron Devices, vol. 55, pp. 2512-2516, // 2008.

[11] A. Tsormpatzoglou, C. A. Dimitriadis, M. Mouis, G. Ghibaudo, and N. Collaert, "Experimental characterization of the subthreshold leakage current in triple-gate FinFETs," Solid-State Electronics, vol. 53, pp. 359-363, // 2009.

[12] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, G. Pananakakis, and R. Clerc, "A compact drain current model of short-channel cylindrical gate-all-around MOSFETs," Semiconductor Science and Technology, vol. 24, // 2009.

[13] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, M. Mouis, G. Ghibaudo, and N. Collaert, "Electrical characterization and design optimization of FinFETs with a TiN/HfO2 gate stack," Semiconductor Science and Technology, vol. 24, // 2009.

[14] E. G. Ioannidis, C. G. Theodorou, A. Tsormpatzoglou, D. H. Tassis, K. Papathanasiou, C. A. Dimitriadis, et al., "Analytical low-frequency noise model in the linear region of lightly doped nanoscale double-gate metal-oxide-semiconductor field-effect transistors," Journal of Applied Physics, vol. 108, // 2010.

[15] E. G. Ioannidis, A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, F. Templier, and G. Kamarinos, "Characterization of traps in the gate dielectric of amorphous and nanocrystalline silicon thin-film transistors by 1/f noise," Journal of Applied Physics, vol. 108, // 2010.

[16] D. H. Tassis, A. Tsormpatzoglou, C. A. Dimitriadis, G. Ghibaudo, G. Pananakakis, and N. Collaert, "Source/drain optimization of underlapped lightly doped nanoscale double-gate MOSFETs," Microelectronic Engineering, vol. 87, pp. 2353-2357, // 2010.

[17] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, G. Pananakakis, and N. Collaert, "Analytical modelling for the current-voltage characteristics of undoped or lightly-doped symmetric double-gate MOSFETs," Microelectronic Engineering, vol. 87, pp. 1764-1768, // 2010.

[18] N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, K. Papathanasiou, J. Jomaah, et al., "Analytical unified threshold voltage model of short-channel FinFETs and implementation," Solid-State Electronics, vol. 64, pp. 34-41, // 2011.

[19] E. G. Ioannidis, A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, and J. Jomaah, "Effect of localized interface charge on the threshold voltage of short-channel undoped symmetrical double-gate MOSFETs," IEEE Transactions on Electron Devices, vol. 58, pp. 433-440, // 2011.

[20] C. G. Theodorou, A. Tsormpatzoglou, C. A. Dimitriadis, S. A. Khan, M. K. Hatalis, J. Jomaah, et al., "Origin of low-frequency noise in the low drain current range of bottom-gate amorphous IGZO thin-film transistors," IEEE Electron Device Letters, vol. 32, pp. 898-900, // 2011.

[21] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, N. Collaert, and G. Pananakakis, "Analytical threshold voltage model for lightly doped short-channel tri-gate MOSFETs," Solid-State Electronics, vol. 57, pp. 31-34, // 2011.

[22] N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, K. Papathanasiou, C. A. Dimitriadis, and G. Ghibaudo, "Compact modeling for the transcapacitances of undoped or lightly doped nanoscale cylindrical surrounding gate MOSFETs," 2012, pp. 953-956.

[23] N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, I. Pappas, K. Papathanasiou, M. Bucher, et al., "Compact capacitance model of undoped or lightly doped ultra-scaled triple-gate FinFETs," IEEE Transactions on Electron Devices, vol. 59, pp. 3306-3312, // 2012.

[24] N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, I. Pappas, K. Papathanasiou, M. Bucher, et al., "Compact model of drain current in short-channel triple-gate FinFETs," IEEE Transactions on Electron Devices, vol. 59, pp. 1891-1898, // 2012.

[25] N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, I. Pappas, K. Papathanasiou, and C. A. Dimitriadis, "Analytical compact modeling of nanoscale triple-gate FinFETs," 2012, pp. 72-75.

[26] N. Hastas, A. Tsormpatzoglou, I. Pappas, D. N. Kouvatsos, D. C. Moschou, A. T. Voutsas, et al., "Trap properties of asymmetrical double-gate polysilicon thin-film transistors with low frequency noise in terms of the grain boundaries direction," 2012, pp. 339-342.

[27] K. Papathanasiou, C. G. Theodorou, A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, M. Bucher, et al., "Symmetrical unified compact model of short-channel double-gate MOSFETs,"

Solid-State Electronics, vol. 69, pp. 55-61, // 2012.

[28] A. Tsormpatzoglou, N. Fasarakis, D. H. Tassis, I. Pappas, K. Papathanasiou, and C. A. Dimitriadis, "Analytical unified drain current model of long-channel tri-gate FinFETs," 2012, pp. 115-118.

[29] A. Tsormpatzoglou, N. A. Hastas, S. Khan, M. Hatalis, and C. A. Dimitriadis, "Comparative study of active-over-metal and metal-over-active amorphous IGZO thin-film transistors with low-frequency noise measurements," IEEE Electron Device Letters, vol. 33, pp. 555-557, // 2012.

[30] A. Tsormpatzoglou, K. Papathanasiou, N. Fasarakis, D. H. Tassis, G. Ghibaudo, and C. A. Dimitriadis, "A Lambert-function charge-based methodology for extracting electrical parameters of nanoscale FinFETs," IEEE Transactions on Electron Devices, vol. 59, pp. 3299-3305, // 2012.

[31] A. Tsormpatzoglou, I. Pappas, D. H. Tassis, C. A. Dimitriadis, and G. Ghibaudo, "Analytical threshold voltage model for short-channel asymmetrical dual-gate material double-gate MOSFETs," Microelectronic Engineering, vol. 90, pp. 9-11, // 2012.

[32] N. Fasarakis, T. A. Karatsori, A. Tsormpatzoglou, D. H. Tassis, K. Papathanasiou, M. Bucher, et al., "Compact Modeling of Nanoscale Trapezoidal FinFETs," IEEE Transactions on Electron Devices, vol. 61, pp. 324-332, // 2014.

[33] D. C. Moschou, C. G. Theodorou, N. A. Hastas, A. Tsormpatzoglou, D. N. Kouvatsos, A. T. Voutsas, et al., "Short channel effects on LTPS TFT degradation," IEEE/OSA Journal of Display Technology, vol. 9, pp. 747-754, // 2013.

[34] A. Tsormpatzoglou, N. A. Hastas, N. Choi, F. Mahmoudabadi, M. K. Hatalis, and C. A. Dimitriadis, "Analytical surface-potential-based drain current model for amorphous InGaZnO thin film transistors," Journal of Applied Physics, vol. 114, // 2013.

[35] A. Tsormpatzoglou, N. A. Hastas, F. Mahmoudabadi, N. Choi, M. K. Hatalis, and C. A. Dimitriadis, "Characterization of high-current stress-induced instability in amorphous InGaZnO thin-film transistors by low-frequency noise measurements," IEEE Electron Device Letters, vol. 34, pp. 1403-1405, // 2013.

[36] Fasarakis, N, D H Tassis, A Tsormpatzoglou, K Papathanasiou, C A Dimitriadis, and G Ghibaudo. 2013. “Compact Modeling of Nano-Scale Trapezoidal Cross-Sectional FinFETs.” In 2013 IEEE International Semiconductor Conference Dresden - Grenoble: Technology, Design, Packaging, Simulation and Test, ISCDG 2013.

[37] A. Tsormpatzoglou, N. A. Hastas, M. K. Hatalis, and C. A. Dimitriadis, "Parameter extraction methodology for amorphous IGZO thin film transistors," in Proceedings of the International Conference on Microelectronics, ICM, 2014, pp. 235-238.

[38] A. Tsormpatzoglou, N. A. Hastas, M. K. Hatalis, and C. A. Dimitriadis, "Analytical unified drain current model of amorphous IGZO thin film transistors considering a Gaussian distribution of tail states," in Proceedings of the International Conference on Microelectronics, ICM, 2014, pp. 269-272.

[39] D. Tassis, I. Messaris, N. Fasarakis, A. Tsormpatzoglou, S. Nikolaidis, and C. Dimitriadis,

"Variability of nanoscale triple gate FinFETs: Prediction and analysis method," in 2014 21st IEEE International Conference on Electronics, Circuits and Systems, ICECS 2014, 2014, pp. 710-713.

[40] A. Tsormpatzoglou, D. H. Tassis, P. Dimitrakis, V. Ioannou-Sougleridis, P. Normand and C. A. Dimitriadis, " Compact Drain Current Model for Nanoscale Junctionless Triple-Gate FinFETs," 12th International Conference on Nanosciences & Nanotechnologies (NN15)

[41] T. A. Karatsori, A. Tsormpatzoglou, C. G. Theodorou, E. G. Ioannidis, S. Haendler, N. Planes, *et al.*, "Analytical Compact Model for Lightly Doped Nanoscale Ultrathin-Body and Box SOI MOSFETs With Back-Gate Control," *IEEE Transactions on Electron Devices*, 2015.

[42] Messaris, I., Fasarakis, N., Karatsori, T.A., Tsormpatzoglou, A., Ghibaudo, G., Dimitriadis, C.A. "Hot carrier degradation modeling of short-channel n-FinFETs" (2015) Device Research Conference - Conference Digest, DRC, 2015-August, art. no. 7175617, pp. 183-184.

[43] Galani, C., Tsormpatzoglou, A., Chaourani, P., Messaris, I., Nikolaidis, S. "A study for replacing CMOS gates by equivalent inverters" (2015) Proceedings - IEEE International Symposium on Circuits and Systems, 2015-July, art. no. 7169014, pp. 1838-1841.

[44] Oproglidis, T.A., Tsormpatzoglou, A., Tassis, D.H., Karatsori, T.A., Barraud, S., Ghibaudo, G., Dimitriadis, C.A. "Analytical Drain Current Compact Model in the Depletion Operation Region of Short-Channel Triple-Gate Junctionless Transistors" IEEE Transactions on Electron Devices, 64 (1), art. no. 7775074, pp. 66-72 // 2017

[45] Oproglidis, T A, A Tsormpatzoglou, C G Theodorou, T A Karatsori, G Ghibaudo, and C A Dimitriadis. 2019. "Upgrade of Drain Current Compact Model for Nanoscale Triple-Gate Junctionless Transistors to Continuous and Symmetric." IEEE Transactions on Electron Devices 66 (10): 4486–89.

[46] Oproglidis, T A, T A Karatsori, C G Theodorou, A Tsormpatzoglou, S Barraud, G Ghibaudo, and C A Dimitriadis. 2020. "Impact of Hot Carrier Aging on the Performance of Triple-Gate Junctionless MOSFETs." IEEE Transactions on Electron Devices 67 (2): 424–29.

[47] Oproglidis, T A, D H Tassis, A Tsormpatzoglou, G Ghibaudo, and C A Dimitriadis. 2020. "Drain Current Local Variability Analysis in Nanoscale Junctionless FinFETs Utilizing a Compact Model." Solid-State Electronics 170: 107835.

[48] Oproglidis, T. A., Karatsori, T. A., Theodorou, C. G., Tsormpatzoglou, A., Barraud, S., Ghibaudo, G., & Dimitriadis, C. A. (2021). Impact of Hot Carrier Aging on the 1/f and Random Telegraph Noise of Short-Channel Triple-Gate Junctionless MOSFETs. *IEEE Transactions on Device and Materials Reliability*, *21*(3), 348–353. https://doi.org/10.1109/TDMR.2021.3094510

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S., Ghibaudo, G., & Dimitriadis, C. A. (2022). Threshold voltage of p-type triple-gate junctionless transistors. *Solid-State Electronics*, *197*. https://doi.org/10.1016/j.sse.2022.108451

[51] Tsormpatzoglou, A., Oproglidis, T. A., Pappas, I., & Dimitriadis, C. A. (2023). Analytical model for the injection recombination current in quantum well micro-light emitting diodes. *Journal of Applied Physics*, *134*(15). https://doi.org/10.1063/5.0171766

Research Interests

My research interests are divided into two main categories:

1. Nanostructure devices for use in optical application systems and
2. Nanoscale MOSFET devices with alternative structures to replace the conventional MOSFET.

The following research categories fall under the first area:

1.1 Electrical measurements and low-frequency noise measurements of nanostructure electronic devices for optical applications.

1.2 Development of analytical and compact current models, electrical measurements, and low-frequency noise measurements of flexible electronics and thin-film transistors (TFTs) for use in flexible displays.

1.3 Modeling and electrical characterization of micro-LED devices with embedded quantum wells.

The following research categories fall under the second area:

2.1 Electrical measurements, reliability measurements, and low-frequency noise measurements of multi-gate MOSFET nanodevices.
2.2 Development of analytical and compact current models for MOSFET nanotransistors.
2.3 Numerical simulations of electronic devices.
2.4 Study of self-heating mechanisms in MOSFET nanotransistors.

Following this, my research interests are presented in detail by category, specifying exactly which research publications and which part of my professional experience (research programs—work in companies) are related to each category.

1.1 Electrical measurements and low-frequency noise measurements of nanostructure electronic devices for optical applications.

This category includes studies related to the electrical characterization of quantum dots embedded in semiconductors (InAs in GaAs and β-FeSi2 in Si). Quantum dots of semiconductor materials, due to their excellent electronic and optical properties, are very promising materials for use in electronic and optoelectronic devices. The InAs quantum dots in GaAs and β-FeSi2 in Si were developed using the molecular beam epitaxy (MBE) technique. Some of the samples were fabricated at the IMEM institute (Italy), and the rest in the laboratory of the Korea Institute of Science and Technology (KIST). To determine the carrier traps caused by the development of the InAs and β-FeSi2 quantum dots within the energy gap of GaAs and Si, respectively, Au/n-GaAs and Au/n-Si Schottky diodes were fabricated as control devices. The electrical characterization was carried out with current-voltage (I-V), capacitance-voltage (C-V), and low-frequency noise measurements at different temperatures. Additionally, silicon carbide (SiC) was studied, which is of great interest for power electronics applications due to its unique physical and electrical properties. I-V, C-V, and low-frequency noise measurements were performed on 4H-SiC p+-n-n+ contacts at room temperature, and the characteristics of the traps at the interfaces and in the

material were determined. This research area corresponds to publications [1-6] and research projects 7 and 9.

1.2 Development of analytical and compact current models, electrical measurements, and low-frequency noise measurements of flexible electronics and thin-film transistors (TFTs) for use in flexible displays.

The revolution that occurred over the past decade with touch screens has naturally led to the development of flexible displays. For the fabrication of flexible displays, transistors are required that can be constructed on flexible films, such as metal surfaces, various polymers, and even paper. InGaZnO appears to be the most promising candidate material for flexible surfaces. InGaZnO transistors were fabricated at the "Display Research Lab" in Bethlehem, USA. I-V, C-V, and low-frequency noise measurements were performed on InGaZnO transistors of various geometries at room temperature, and the characteristics of the traps at the interfaces and in the material were determined. Furthermore, DC and AC electrical stress measurements were conducted. To comprehensively study InGaZnO TFTs, analytical models were developed for the transistor channel currents. The models were validated using experimental devices developed at Lehigh University (Bethlehem, PA, USA) and TCAD simulations. This research area corresponds to publications [20], [26], [29], [34], [37], [38], [49-50], and research project 5.

1.3 Modeling and electrical characterization of micro-LED devices with embedded quantum wells.

As part of the ongoing revolution in the field of virtual reality, the optimization of LED performance is critically important. The most promising new technology is that of micro-LEDs with embedded quantum wells. As the dimensions of LEDs shrink, new challenges arise regarding their mass production, the electrical characterization of the new devices, and the development of models that describe their electrical behavior and, consequently, their overall performance. In collaboration with the world leader Oculus, acquired by FACEBOOK, a direct assignment project was undertaken to study various micro-LED technologies. For the first time, compact and analytical current models were developed for the three colors of diodes: red, green, and blue. Additionally, simulations of the devices were performed using TCAD simulation tools.

Since this research on these devices is confidential and concerns technologies exclusively held by the sponsor company, under the signed NDA, the only publishable work after an appropriate period is publication [51]. This research area corresponds to research projects 1 and 2.

2.1 Electrical measurements, reliability measurements, and low-frequency noise measurements of multi-gate MOSFET nanodevices.

As technology demands the continuous miniaturization of transistor dimensions, multi-gate MOSFETs promise to function well even at dimensions of a few nanometers. The samples were measured at the IMEP-LAHC laboratory in Grenoble, France, at the MINATEC research center, and were fabricated by the IMEC research center (Belgium). These are triple-gate MOSFETs (FinFETs) with gate lengths down to 40 nm. The use of multiple gates helps avoid short-channel effects, which reduce gate control within the channel and degrade the main operating and performance characteristics of the transistors. Measurements were performed on the SussMicroTecLT probe station using the HP 4155 semiconductor parameter analyzer. In addition to characterizing the samples through input and output measurements, capacitance measurements (CV-SPLIT) were also conducted. Experience was gained with advanced systems for temperature control under high vacuum, impedance, and noise measurements. To characterize the measurements, 3D simulation programs from Silvaco (Devedit3D and Atlas3D) were used. This research area corresponds to publications [11], [13], [15], [16], [48], and research projects 3, 4, and 8.

2.2 Development of analytical and compact current models for MOSFET nanotransistors.

This research area includes studies related to the development of analytical and compact current models that accurately describe the main characteristics of small-dimension transistors. The classical models used until now are unable to predict the behavior of devices when the channel length is reduced to a few nanometers, as phenomena arise solely due to the reduction in dimensions. Analytical models have the dual advantage of simplicity, making them useful in circuit simulation tools, and being directly linked to specific physical processes.
It is widely believed that one of the best candidate devices to replace current technology, which cannot cope with the reduction in dimensions, is multi-gate MOSFET transistors. Starting with

the simplest case, that of the double-gate MOSFET, we developed analytical models for potential distributions for triple-gate transistors (FinFETs) and four-gate transistors (circular and square cross-sections), trapezoidal channels, as well as other technological peculiarities, such as junctionless three-gate transistors with a high channel concentration. These efforts led to analytical models for the threshold voltage, subthreshold slope, drain-induced barrier lowering (DIBL), input and output currents, and channel capacitances. Fully-depleted SOI MOSFETs (FD-SOI MOSFETs) manufactured at ST Microelectronics in Grenoble, France, were also studied. Their uniqueness lies in the ultra-thin silicon film, approximately 10 nanometers thick, deposited on a silicon dioxide film, which in turn is deposited on a highly doped silicon substrate connected to an additional bias. The extra bias acts as a second gate for the transistor, allowing for control of the threshold voltage and all the electrical properties of the transistor.
For FD-SOI MOSFETs, the same research practices applied to multi-gate transistors were followed. To verify the models, 3D simulation programs from Silvaco (Devedit3D and Atlas3D) and finite element analysis were used. This research area corresponds to publications [7-9], [10], [12], [14], [17-19], [21-25], [27-28], [30-32], [36], [40-41], and [44], and research projects 3, 4, 6, and 8.

2.3 Numerical simulations of electronic devices.

In all cases where analytical models were developed, to certify them, in addition to comparing them with experimental measurements, they also needed to be compared with simulations. For publications [7-10], the program used was FLEXPDE, a differential equation solver using finite element analysis, with expertise acquired at the IMEP-LAHC laboratory. For the other published works, the TCAD Silvaco ATLAS tool was used.

2.4 Study of self-heating mechanisms in MOSFET nanotransistors.

In my work at CEA-LETI, I conducted extensive self-heating measurements on nanoscale FD-SOI MOSFETs using the gate resistance thermometry (GRT) method. The transistors were specially developed and modified by ST Microelectronics (Grenoble, France) to study the change in gate resistance when the transistor was in operation. Additionally, measurements were performed to assess the effect of self-heating on the surrounding environment of the transistor, to

investigate the heat dissipation in the circuit and the potential impact of the phenomenon on the circuit's operation.